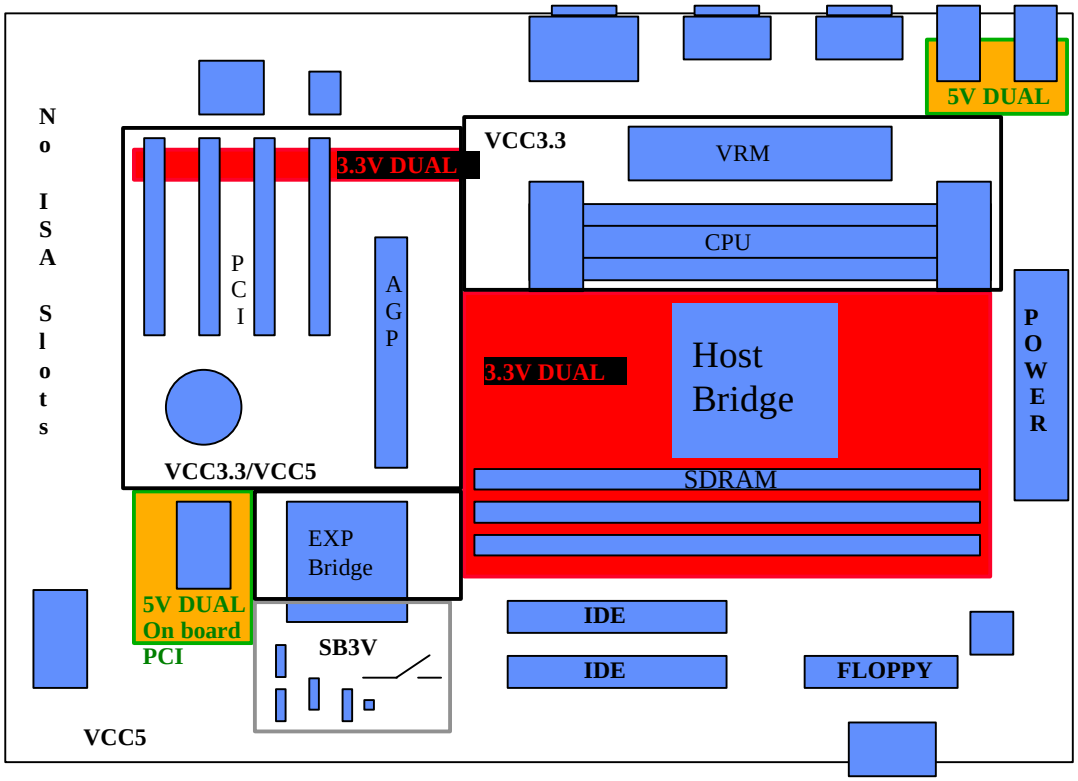
Instantly Available PC
FETs on Motherboard
3.3Vdual Implementation

Gary Solomon
Jerzy Kolinski

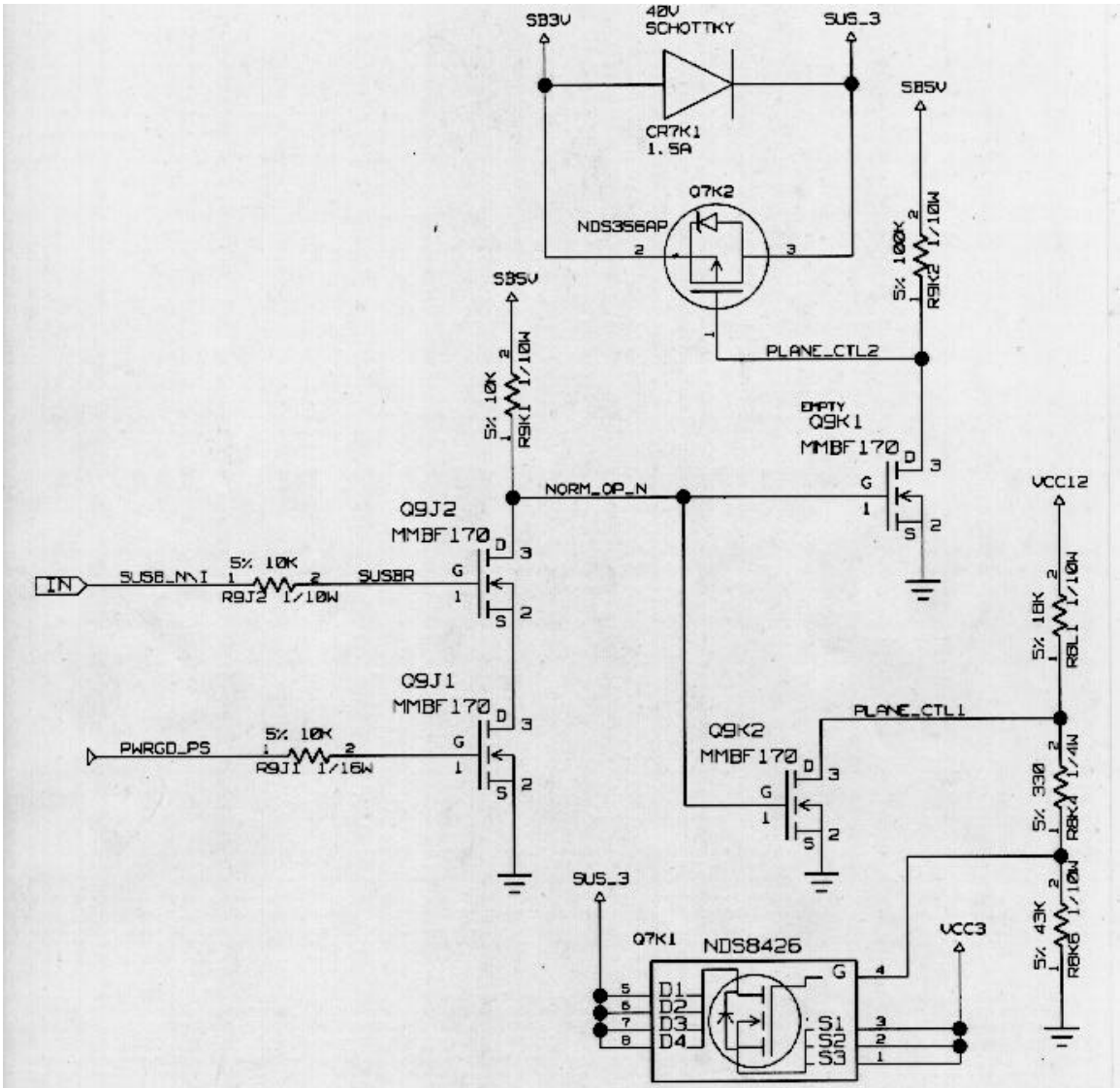
Intel - Platform Architecture Lab

Building an Instantly Available PC involve split plane design which enables certain portions of the system to remain powered while the bulk of the system is powered off. (i.e. DRAM self-refresh, and 3.3Vaux remain active during S3). The following picture illustrates the split power plane partitioning utilized in the PAL design. Note that the minimum implementation provides support only for the 3.3Vdual voltage output which supports the DRAM, DRAMC, and 3.3Vaux PCI slot supply voltage. 5Vdual would need to be provided if S3 support for USB devices, or other motherboard 5Volt devices is desired.



The circuit below details what the Platform Architecture Lab team mated to a standard NLX power supply to construct the 3.3Vdual output (Instantly Available PCs based upon fully integrated dual mode power supplies were also built). This circuit sources power for the DRAM plane, as well as the 3.3Vaux PCI connector pins.

Note that a fully integrated dual mode power supply (refer to the Instantly Available PC Power Delivery spec, and Instantly Available PC Design Guide) may prove to be the best overall solution long term, however the distributed solution described here may enable the quickest time to market.



Circuit Description:

Control signals:

There are two control signals for the FET circuit: Susb# from the PIIX4 and Power_good from the power supply. Susb# indicates when the system is entering the ACPI S3 state. The power good signal is used as qualifier to ensure that power rails from the power supply are at the valid voltage levels.

During normal (working state) operation both control signals are at a high voltage level which cuts off the P- channel FET (Q7k2). High power FET (Q7K1) routes the runtime (high capacity) current to the memory plane. This FET is rated at 8 Amps.

When the system goes to S3 the Susb# signal is activated, i.e. transitions from high to low. Also the Power_good signal from the power supply transitions to the low state. When both signals are low the main (working state) FET (Q7K1) is cut off and the P-channel (sleep state) FET routes the standby converter current to the memory plane.

Maintaining regulation through transitions between Main and Auxiliary converters:

For the PAL Instantly Available PC implementation (with a beta Win98 OS) maintaining regulation prior to transitioning to the standby converter (S3) was not an issue. (i.e. the platform was at ~30W from the wall just prior to switching over to the aux power converter). Analysis needs to be done at platform design/integration time (once baseline feature components and their PM capabilities are known) to determine what the lightest possible instrumented load could be while the main converter is active in order to determine whether some form of surrogate transitional load would be required.

Additionally, enough de-coupling capacitors need to be added to the DRAM array to ensure that the voltage regulation specs (i.e. the SDRAM DC characteristics specification) are not violated during transitions between the converters.